

SPECIFICATION

METHOD OF CONTROLLING IMAGE DISPLAY

5

TECHNICAL FIELD

The present invention relates to an image display apparatus control method and, more particularly, to a power-on/off control method and emergency shutdown control method for an image display apparatus using an image display panel having a multi electron source on which a plurality of cold cathode devices are wired in a matrix, and fluorescent substances for emitting light upon irradiation with an electron beam from each cold cathode device.

15

BACKGROUND ART

Conventionally, two types of devices, namely a thermionic cathode device and cold cathode device, are known as electron-emitting devices. Known examples of the cold cathode devices are surface-conduction type emitting devices, field emission type emitting devices (to be referred to as FE type emitting devices hereinafter), and metal/insulator/metal type emitting devices (to be referred to as MIM type emitting devices hereinafter).

As surface-conduction type emitting devices, e.g., 25 M.I. Elinson, Radio Eng. Electron Phys., 10, 1290 (1965) and other examples (to be described later) are known.

The surface-conduction type emitting device utilizes the phenomenon that electrons are emitted by flowing a current through a small-area thin film formed on a substrate in parallel with the film surface. The surface-conduction 5 type emitting device includes an emitting device using an Au thin film [G. Dittmer, "Thin Solid Films", 9, 317 (1972)], an emitting device using an In_2O_3/SnO_2 thin film [M. Hartwell and C.G. Fonstad, "IEEE Trans. ED Conf.", 519 (1975)], an emitting device using a carbon thin film [Hisashi Araki et 10 al., "Vacuum", Vol. 26, No. 1, p. 22 (1983)], and the like, in addition to an emitting device using an SnO_2 thin film by Elinson et al.

Fig. 28 is a plan view showing the device by M. Hartwell et al. described above as a typical example of the 15 device structures of these surface-conduction type emitting devices. In Fig. 28, reference numeral 3001 denotes a substrate; and 3004, a conductive thin film made of a metal oxide formed by sputtering. The conductive thin film 3004 has an H-shaped flat pattern, as shown in Fig. 28. 20 The conductive thin film 3004 undergoes electrification processing (to be referred to as forming processing), thereby forming an electron-emitting portion 3005. An interval L in Fig. 28 is set to 0.5 to 1 [mm], and W is set to 0.1 [mm]. The electron-emitting portion 3005 is 25 illustrated in a rectangular shape at the center of the conductive thin film 3004 for the sake of illustrative

convenience. However, this does not exactly show the actual position and shape of the electron-emitting portion.

In the above surface-conduction type emitting devices by M. Hartwell et al. and the like, typically the 5 electron-emitting portion 3005 is formed by performing electrification processing called forming processing for the conductive thin film 3004 before electron emission. In electrification forming, a constant DC voltage or a DC voltage which rises at a very low rate of, e.g., about 1 10 V/min is applied across the conductive thin film 3004 to locally destroy, deform or denature the conductive thin film 3004, thereby forming the electron-emitting portion 3005 with an electrically high resistance. Note that the locally destroyed, deformed or denatured part of the 15 conductive thin film 3004 has a fissure. When an appropriate voltage is applied to the conductive thin film 3004 after electrification forming, electrons are emitted near the fissure.

Known examples of the FE type devices are described 20 in W.P. Dyke and W.W. Dolan, "Field emission", Advance in Electron Physics, 8, 89 (1956) and C.A. Spindt, "Physical properties of thin-film field emission cathodes with molybdenum cones", J. Appl. Phys., 47, 5248 (1976).

Fig. 29 is a sectional view showing the device by C.A. 25 Spindt et al. described above as a typical example of the FE type device structure. In Fig. 29, reference numeral

3010 denotes a substrate; 3011, an emitter wiring line made of a conductive material; 3012, an emitter cone; 3013, an insulating layer; and 3014, a gate electrode. This device is caused to produce a field emission from the tip of the 5 emitter cone 3012 by applying an appropriate voltage between the emitter cone 3012 and the gate electrode 3014.

As another FE type device structure, there is an example in which an emitter and gate electrode are arranged on a substrate to be almost parallel to the substrate 10 surface, instead of the multilayered structure of Fig. 29.

A known example of the MIM type emitting devices is described in C.A. Mead, "Operation of tunnel-emission Devices, J. Appl. Phys., 32, 646 (1961).

Fig. 30 shows a typical example of the MIM type device 15 structure. Fig. 30 is a sectional view. Reference numeral 3020 denotes a substrate; 3021, a lower metal electrode; 3022, a thin insulating layer having a thickness of about 100 Å; and 3023, an upper metal electrode having a thickness of about 80 to 300 Å. The MIM type emitting 20 device emits electrons from the surface of the upper electrode 3023 by applying an appropriate voltage between the upper electrode 3023 and the lower electrode 3021.

Since these cold cathode devices can emit electrons at a lower temperature, compared to the thermionic cathode 25 devices, the cold cathode devices do not require any heater. The cold cathode device has a structure simpler than that

of the thermionic cathode device, and it is possible to fabricate elements that are finer. Even if many devices are arranged on a substrate at a high density, problems such as heat fusion of the substrate hardly arise. In addition, 5 the response speed of the cold cathode device is high, while the response speed of the thermionic cathode device is low because it operates upon heating by a heater.

For this reason, applications of the cold cathode devices have enthusiastically been studied.

10 Of cold cathode devices, the surface-conduction type emitting device has a simple structure and can be easily manufactured to allow forming many devices on a wide area. As disclosed in Japanese Patent Laid-Open No. 64-31332 filed by the present applicant, a method of arranging and 15 driving many devices has been studied.

Regarding applications of the surface-conduction type emitting devices to, e.g., image forming apparatuses such as image display apparatuses and image recording apparatuses, charge beam sources, and the like have been 20 studied.

Particularly as an application to image display apparatuses, as disclosed in the USP 5,066,883 and Japanese Patent Laid-Open Nos. 2-257551 and 4-28137 filed by the present applicant, an image display apparatus using a 25 combination of surface-conduction type emitting devices and fluorescent substances which emit light upon

irradiation with an electron beam has been studied. This type of image display apparatus using a combination of surface-conduction type emitting devices and fluorescent substances is expected to exhibit more excellent
5 characteristics than other conventional image display apparatuses. For example, compared with recent popular liquid crystal display apparatuses, the above display apparatus is superior in that it does not require any backlight because of a self-emission type and that it has
10 a wide view angle.

A method of driving many FE type emitting devices arranged side by side is disclosed in, e.g., USP 4,904,895 filed by the present applicant. As a known example of an application of FE type emitting devices to an image display
15 apparatus is a flat display apparatus reported by R. Meyer et al. [R. Meyer: "Recent Development on Microtips Display at LETI", Tech. Digest of 4th Int. Vacuum Microelectronics Conf., Nagahama, pp. 6 - 9 (1991)].

An example of an application of many MIM type emitting devices arranged side by side to an image display apparatus is disclosed in Japanese Patent Laid-Open No. 3-55738 filed
20 by the present applicant.

The present inventors have examined cold cathode devices of various materials, manufacturing methods, and
25 structures, in addition to the prior arts. Further, the present inventors have made extensive studies on a multi

electron beam source having many cold cathode devices, and an image display apparatus using this multi electron beam source.

Fig. 31 shows a multi electron beam source by an electrical wiring method examined by the present inventors. More specifically, this multi electron beam source is constituted by two-dimensionally arranging many cold cathode devices, and wiring these devices in a matrix, as shown in Fig. 31. In Fig. 31, reference numeral 4001 denotes a schematic cold cathode device; 4002, a row-direction wiring line; and 4003, a column-direction wiring line. In practice, the row-direction wiring line 4002 and column-direction wiring line 4003 have finite electrical resistances, which are represented as wiring resistances 4004 and 4005 in Fig. 31. This wiring method is called a simple matrix wiring method.

For the illustrative convenience, the multi electron beam source is illustrated in a 6 x 6 matrix, but the size of the matrix is not limited to this. For example, in a multi electron beam source for an image display apparatus, devices enough to display a desired image are arranged and wired.

In a multi electron beam source in which cold cathode devices are wired in a simple matrix, appropriate electrical signals are applied to the row-direction wiring line 4002 and column-direction wiring line 4003 in order

to output a desired electron beam. For example, to drive cold cathode devices on an arbitrary row in the matrix, a selection voltage V_s is applied to the row-direction wiring line 4002 on the row to be selected, and at the same time 5 a non-selection voltage V_{ns} is applied to the row-direction wiring lines 4002 on unselected rows. In synchronism with this, a driving voltage V_e for outputting an electron beam is applied to the column-direction wiring lines 4003. According to this method, so long as voltage drops across 10 the wiring resistances 4004 and 4005 are neglected, a voltage $V_e - V_s$ is applied to cold cathode devices on the selected row, and a voltage $V_e - V_{ns}$ is applied to cold cathode devices on the unselected rows. If the voltages 15 V_e , V_s , and V_{ns} are set to appropriate levels, an electron beam having a desired intensity must be output from only cold cathode devices on the selected row. If different driving voltages V_e are applied to respective column-direction wiring lines, electron beams having different intensities must be output from respective 20 devices on the selected row. If the application time of the driving voltage V_e is changed, the electron beam output time must be changed.

Hence, a multi electron beam source having cold cathode devices wired in a simple matrix can be applied for 25 variety purposes. For example, if an electrical signal corresponding to image information is properly applied, the

multi electron beam source can be preferably used as an electron source for an image display apparatus.

In practice, however, the multi electron beam source having cold cathode devices wired in a simple matrix suffers 5 the following problems.

When the power source of the image display apparatus is turned on, before outputs to be applied from voltage power sources to row-direction wiring lines and column-direction wiring lines stabilize, the outputs from 10 the power sources are applied to the multi electron beam source to damage cold cathode devices.

The same phenomenon occurs when the power source is turned off.

When the potential difference between an acceleration potential for accelerating electrons from the electron source and a potential supplied to the electron source in order to emit electrons is large, and particularly when the potential difference between the electron emission potential and the acceleration potential is 500 V or more, 20 3 kv or more, or 5 kV or more, an unexpected power source operation may occur while a high acceleration potential is applied. In this case, a discomfort display state may be generated, or the performance of the display panel such as the characteristics of the fluorescent substance may be 25 influenced.

It is an object of an invention according to the

present application to improve the display state and reduce damage to the image display apparatus when a power source is turned on, the power source is turned off, an outlet is removed, or power fails.

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DISCLOSURE OF INVENTION

According to one invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a modulation circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping the output from the modulation circuit to the display panel until the signal output from the modulation circuit to the display panel is determined.

According to another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a modulation circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, delaying the output of the signal from the modulation circuit to the display panel after a power source is turned on, and determining the signal output from the modulation circuit to the display panel during the delay time.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a modulation circuit

5 to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping application of an acceleration potential for accelerating electrons from the electron source until the signal output from the modulation circuit

10 to the display panel is determined.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a modulation circuit

15 to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, delaying application of an acceleration potential for accelerating electrons from the electron source after a power source is turned on, and determining

20 the signal output from the modulation circuit to the display panel during the delay time.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a scanning circuit to

25 a display panel for displaying an image by irradiation with

electrons from an electron source to fluorescent substances, stopping the output from the scanning circuit to the display panel until the signal output from the scanning circuit to the display panel is determined.

5 According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a scanning circuit to a display panel for displaying an image by irradiation with 10 electrons from an electron source to fluorescent substances, delaying the output of the signal from the scanning circuit to the display panel after a power source is turned on, and determining the signal output from the scanning circuit to the display panel during the delay time.

15 According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a scanning circuit to a display panel for displaying an image by irradiation with 20 electrons from an electron source to fluorescent substances, stopping application of an acceleration potential for accelerating electrons from the electron source until the signal output from the scanning circuit to the display panel is determined.

25 According to still another invention of the present application, an image display apparatus control method is

characterized by comprising, when image display is to be started by outputting a signal from a scanning circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances,

5 delaying application of an acceleration potential for accelerating electrons from the electron source after a power source is turned on, and determining the signal output from the scanning circuit to the display panel during the delay time.

10 According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a modulation circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping the output from the modulation circuit to the display panel until a power source voltage of the modulation circuit reaches a desired value.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a modulation circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, delaying the output of the signal from the modulation circuit to the display panel after a power source

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is turned on, and setting a power source voltage of the modulation circuit to a desired value during the delay time.

According to still another invention of the present application, an image display apparatus control method is 5 characterized by comprising, when image display is to be started by outputting a signal from a modulation circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping application of an acceleration 10 potential for accelerating electrons from the electron source until a power source voltage of the modulation circuit reaches a desired value.

According to still another invention of the present application, an image display apparatus control method is 15 characterized by comprising, when image display is to be started by outputting a signal from a modulation circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, delaying application of an acceleration 20 potential for accelerating electrons from the electron source after a power source is turned on, and setting a power source voltage of the modulation circuit to a desired value during the delay time.

According to still another invention of the present 25 application, an image display apparatus control method is characterized by comprising, when image display is to be

started by outputting a signal from a scanning circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping the output from the scanning circuit to the display 5 panel until a power source voltage of the scanning circuit reaches a desired value.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be 10 started by outputting a signal from a scanning circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, delaying the output of the signal from the scanning circuit to the display panel after a power source is turned on, and 15 setting a power source voltage of the scanning circuit to a desired value during the delay time.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be 20 started by outputting a signal from a scanning circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping application of an acceleration potential for accelerating electrons from the electron source until a 25 power source voltage of the scanning circuit reaches a desired value.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when image display is to be started by outputting a signal from a scanning circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, delaying application of an acceleration potential for accelerating electrons from the electron source after a power source is turned on, and setting a power source voltage of the scanning circuit to a desired value during the delay time.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when a power source is to be turned off while an image is displayed by outputting a signal from a modulation circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping the output of the signal from the modulation circuit to the display panel, and then stopping supply of power to the modulation circuit.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when a power source is to be turned off while an image is displayed by outputting a signal from a scanning circuit to a display panel for

displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping the output of the signal from the scanning circuit to the display panel, and then stopping supply of power to the 5 scanning circuit.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when emergency shutdown is to be performed while an image is displayed by outputting a 10 signal from a modulation circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping the output of the signal from the modulation circuit to the display panel, and then stopping supply of power to the 15 modulation circuit.

According to still another invention of the present application, an image display apparatus control method is characterized by comprising, when emergency shutdown is to be performed while an image is displayed by outputting a 20 signal from a scanning circuit to a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, stopping the output of the signal from the scanning circuit to the display panel, and then stopping supply of power to the 25 scanning circuit.

According to still another invention of the present

application, an image display apparatus control method is characterized by comprising, when a voltage abnormality is observed while an image is displayed by outputting a signal from a modulation circuit to a display panel for displaying 5 an image by irradiation with electrons from an electron source to fluorescent substances, stopping the output of the signal from the modulation circuit to the display panel, and then stopping supply of power to the modulation circuit.

According to still another invention of the present 10 application, an image display apparatus control method is characterized by comprising, when a voltage abnormality is observed while an image is displayed by outputting a signal from a scanning circuit to a display panel for displaying an image by irradiation with electrons from an electron 15 source to fluorescent substances, stopping the output of the signal from the scanning circuit to the display panel, and then stopping supply of power to the scanning circuit.

The power is preferably supplied from an auxiliary power source in performing control when the voltage 20 abnormality is observed.

In each of the above-described inventions, a time during which the signal output to the display panel is stopped, or a time during which application of the acceleration potential is stopped, or the delay time is a 25 predetermined time. The predetermined time is selected by counting a predetermined number of sync signals, or

obtained by counting the predetermined time with a timer.

Each invention can be preferably employed especially when the electron source comprises a plurality of row-direction wiring lines for receiving a scanning signal, 5 a plurality of column-direction wiring lines for receiving a modulation signal, and a plurality of electron-emitting devices connected to the row-direction wiring lines and the column-direction wiring lines.

Each invention can be preferably employed especially 10 when the acceleration potential for accelerating electrons from the electron source is a potential higher by not less than 500 V than a potential applied to emit electrons in the electron source. In this case, the potential applied to emit electrons in the electron source is, e.g., a 15 potential applied to an electron-emitting portion. For example, in an electron-emitting device which receives a potential difference between electrodes to emit electrons, the potential applied to emit electrons is a lower potential applied to the one of the electrodes which receive the 20 potential difference.

According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to 25 fluorescent substances, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit

for supplying a modulation signal to the display panel, and a control circuit for stopping output from the scanning circuit and/or the modulation circuit to the display panel until a signal output from the scanning circuit and/or the 5 modulation circuit to the display panel is determined in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel.

According to still another invention of the present 10 application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit 15 for supplying a modulation signal to the display panel, and a control circuit for delaying output of a signal from the scanning circuit and/or the modulation circuit to the display panel after a power source is turned on in starting image display by outputting a signal from the scanning 20 circuit and/or the modulation circuit to the display panel, wherein the signal output from the scanning circuit and/or the modulation circuit to the display panel is determined during the delay time.

According to still another invention of the present 25 application, an image display apparatus is characterized by comprising a display panel for displaying an image by

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irradiation with electrons from an electron source to fluorescent substances, an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit for supplying a modulation signal to the display panel, and a control circuit for stopping supply of the acceleration potential until a signal output from the scanning circuit and/or the modulation circuit to the display panel is determined in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel.

According to still another invention of the present
15 application, an image display apparatus is characterized
by comprising a display panel for displaying an image by
irradiation with electrons from an electron source to
fluorescent substances, an acceleration potential supply
circuit for supplying to the display panel an acceleration
20 potential for accelerating electrons from the electron
source, a scanning circuit for supplying a scanning signal
to the display panel, a modulation circuit for supplying
a modulation signal to the display panel, and a control
circuit for delaying supply of the acceleration potential
25 after a power source is turned on in starting image display
by outputting a signal from the scanning circuit and/or the

modulation circuit to the display panel, wherein the signal output from the scanning circuit and/or the modulation circuit to the display panel is determined during the delay time.

5 According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit for supplying a modulation signal to the display panel, and a control circuit for stopping output from the scanning circuit and/or the modulation circuit to the display panel until a power source voltage of the scanning circuit and/or 10 the modulation circuit reaches a desired value in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel.

15

According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit for supplying a modulation signal to the display panel, and 20 a control circuit for delaying output of a signal from the scanning circuit and/or the modulation circuit to the 25

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display panel after a power source is turned on in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel, wherein a power source voltage of the scanning circuit and/or the modulation circuit reaches a desired value during the delay time.

According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit for supplying a modulation signal to the display panel, and a control circuit for stopping supply of the acceleration potential until a power source voltage of the scanning circuit and/or the modulation circuit reaches a desired value in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel.

According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, an acceleration potential supply

5 circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit for supplying a modulation signal to the display panel, and a control circuit for delaying supply of the acceleration potential after a power source is turned on in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel, wherein a power source voltage of the scanning circuit and/or the modulation circuit reaches a desired value during the delay time.

10 According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit for supplying a modulation signal to the display panel, and a control circuit for stopping output of a signal from the scanning circuit and/or the modulation circuit to the display panel, and then stopping supply of power to the scanning circuit and/or the modulation circuit in turning off a power source

while an image is displayed by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel.

According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit for supplying a modulation signal to the display panel, and a control circuit for stopping output of a signal from the scanning circuit and/or the modulation circuit to the display panel, and then stopping supply of power to the scanning circuit and/or the modulation circuit in performing emergency shutdown while an image is displayed by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel.

According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by irradiation with electrons from an electron source to fluorescent substances, an acceleration potential supply circuit for supplying to the display panel an acceleration

potential for accelerating electrons from the electron source, a scanning circuit for supplying a scanning signal to the display panel, a modulation circuit for supplying a modulation signal to the display panel, and a control 5 circuit for stopping output of a signal from the scanning circuit and/or the modulation circuit to the display panel, and then stopping supply of power to the scanning circuit and/or the modulation circuit when a voltage abnormality is observed while an image is displayed by outputting a 10 signal from the scanning circuit and/or the modulation circuit to the display panel.

According to still another invention of the present application, an image display apparatus is characterized by comprising a display panel for displaying an image by 15 irradiation with electrons from an electron source to fluorescent substances, an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source, a scanning circuit for supplying a scanning signal 20 to the display panel, a modulation circuit for supplying a modulation signal to the display panel, a first power source for supplying power to the acceleration potential supply circuit and/or the scanning circuit and/or the modulation circuit, and a second power source for supplying 25 power to the scanning circuit and/or the modulation circuit upon an abnormal state. In this case, the abnormal state

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is emergency shutdown, and the second power source comprises a capacitor or a battery.

Each of the above-described inventions does not exclude an arrangement in which the scanning circuit and/or 5 the modulation circuit and/or the acceleration potential supply circuit also serves as the control circuit.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a block diagram showing the driving circuit 10 of an image display apparatus;

Fig. 2 is a block diagram showing an NTSC-RGB decoder unit;

Fig. 3 is a block diagram showing an analog processing unit;

15 Fig. 4 is a block diagram showing another arrangement of the first embodiment;

Fig. 5 is a timing chart for explaining the operation of a display panel driving circuit;

Fig. 6 is a block diagram showing a power source line 20 layout;

Fig. 7 is a block diagram showing the flow of a control signal for controlling supply of power;

Fig. 8 is a circuit diagram showing a power source circuit and power source monitoring circuit;

25 Fig. 9 is a flow chart according to the first embodiment;

Fig. 10 is a flow chart according to the second embodiment;

Fig. 11 is a flow chart according to the third embodiment;

5 Fig. 12 is a flow chart according to the fourth embodiment;

Fig. 13 is a flow chart according to the fifth embodiment;

10 Fig. 14 is a flow chart according to the sixth embodiment;

Fig. 15 is a flow chart according to the seventh embodiment;

Fig. 16 is a perspective view showing a display panel;

15 Fig. 17 shows views of the layouts of fluorescent substances;

Fig. 18 shows a plan view and sectional view of a flat surface-conduction type electron-emitting device;

20 Fig. 19 shows sectional views of the steps in manufacturing a flat surface-conduction type electron-emitting device;

Fig. 20 is a waveform chart showing a forming voltage;

25 Fig. 21 shows waveform charts of an application voltage for electrification activation processing;

Fig. 22 is a sectional view showing a stepped

surface-conduction type electron-emitting device;

Fig. 23 shows sectional views of the steps in manufacturing a stepped surface-conduction type electron-emitting device;

5 Fig. 24 is a graph showing the characteristics of an electron-emitting device;

Fig. 25 is a plan view showing a multi electron beam source;

10 Fig. 26 is a sectional view showing the multi electron beam source taken along the line B - B';

Fig. 27 is a block diagram showing a multifunctional display panel;

Fig. 28 is a plan view showing a conventional surface-conduction type electron-emitting device;

15 Fig. 29 is a sectional view showing a conventional field emission type electron-emitting device;

Fig. 30 is a sectional view showing a conventional MIM type electron-emitting device; and

20 Fig. 31 is a circuit diagram showing the layout of electron-emitting devices that has been examined by the present inventor to find a problem.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The best mode for carrying out the present invention 25 will be described with reference to the accompanying drawings.

[First Embodiment]

Fig. 1 is a block diagram showing a driving circuit for an SED (Surface Electron emitter Display) panel according to this embodiment.

Reference symbol P2000 denotes a display panel. In this embodiment, the display panel P2000 is constituted by arranging 240*720 surface-conduction type devices; P2001 in a matrix by row wiring lines of 240 vertical rows and column wiring lines of 720 horizontal columns. An electron beam emitted by each surface-conduction type device; P2001 is accelerated by a high voltage applied from a high-voltage power source unit; P30 to irradiate fluorescent substances (not shown), thereby emitting light. The fluorescent substance (not shown) can take various color layouts in accordance with application purposes. For example, the fluorescent substance takes a vertically striped color layout of R, G, and B colors.

This embodiment will exemplify an application of displaying an NTSC television image on a display panel having pixels of 240 horizontal (R, G, and B trio) * 240 vertical lines. Almost the same arrangement can cope with not only the NTSC image but also image signals having different resolutions and frame rates, such as a high-resolution HDTV image and computer output image.

The driving circuit for the SED (Surface Electron emitter Display) panel is constituted by a video circuit

unit, system control unit, and driving circuit unit.

Reference symbol P1 shown in Fig. 2 denotes an NTSC-RGB decoder unit for receiving an NTSC composite video input and outputting R, G, and B components. This unit 5 separates and outputs a sync signal (SYNC) superposed on an input video signal. Similarly, the unit separates a color burst signal superposed on the input video signal, and generates and outputs a CLK signal (CLK1) which synchronizes with the color burst signal.

Reference symbol P2 shown in Fig. 3 denotes a timing generation unit for generating timing signals necessary for converting analog R, G, and B signals decoded by P1 into digital tone level signals for modulating the luminance of the SED panel. This timing signal includes a clamp pulse 10 for DC-regenerating R, G, and B analog signals from P1 by analog processing units; P3, a blanking pulse (BLK pulse) for adding blanking periods to the R, G, and B analog signals from P1 by the analog processing units; P3, a detection pulse for detecting the levels of the R, G, and B analog 15 signals by video detection units; P4, a sample pulse (not shown) for converting the analog R, G, and B signals into digital signals by A/D units; P6, a RAM controller control signal necessary for a RAM controller; P12 to control RAMs; P8, a free-running CLK signal (CLK2) which is generated in 20 P2 and synchronizes with CLK1 from the internal PLL circuit of P2 when P2 receives CLK1, and a sync signal (SYNC2) 25

generated in P2 based on CLK2. The timing generation unit; P2 having the free-running CLK2 generation means can generate CLK2 and SYNC2 serving as reference signals even when no input video signal exists, and thus an image can 5 be displayed by reading out image data in the RAM means; P8.

P3 shown in Fig. 4 is the analog processing units disposed for respective primary color signals from P1. The analog processing unit P3 mainly performs the following 10 operation. The analog processing unit P3 receives a clamp pulse from P2, and performs DC regeneration. P3 receives a BLK pulse from P2, and adds a blanking period. P3 receives a gain adjustment signal from a corresponding D/A unit; P14 serving as one of control outputs of a system control unit 15 mainly made up of a MPU; P11, and controls the amplitude of a primary color signal input from P1. P3 receives an offset adjustment signal from the D/A unit; P14 serving as one of control outputs of the system control unit mainly made up of the MPU; P11, and controls the black level of 20 a primary color signal input from P1.

Reference numerals P4 denote the video detection units for detecting input video signal levels or image signal levels after control by the analog processing units; P3. Each P4 receives a detection pulse from P2, and the 25 detection result is read by a corresponding A/D unit; P15 serving as one of control inputs of the system control unit

mainly made up of the MPU; P11.

The detection pulse from P2 is formed from, e.g., three, gate pulse, reset pulse, and sample & hold (to be referred to as S/H hereinafter) pulse. The video detection 5 unit is comprised of, e.g., an integrating circuit and S/H circuit.

For example, the integrating circuit integrates a video signal in accordance with a gate pulse during the effective period of an input video signal, and the S/H 10 circuit samples an output from the integrating circuit in accordance with an S/H pulse generated during a vertical blanking period. The detection result is read by the A/D unit; P15 during this vertical blanking period, and then the integrating circuit and S/H circuit are initialized by 15 a reset pulse.

This operation enables detecting the average video level of each field.

Each FPE; P5 is a pre-filter means arranged on the input stage of a corresponding A/D unit; P6.

20 The A/D unit; P6 is an A/D converter means for receiving a sample CLK from P2 and quantizing an analog primary color signal having passed through the LPF; P5 by a necessary number of tone levels.

Each inverse γ table; P7 is a tone level 25 characteristic conversion means adopted to convert an input video signal into the emission characteristic of the

display panel. When the luminance level is expressed by pulse width modulation, like this embodiment, the emission amount often exhibits a linear characteristic almost proportional to the size of luminance data. On the other 5 hand, a video signal applies to a TV receiver using a CRT, and undergoes γ processing in order to correct the nonlinear emission characteristic of the CRT. For this reason, in displaying a TV image on a panel having a linear emission characteristic, like this embodiment, the effects 10 of γ processing must be canceled by a tone level characteristic conversion means such as P7.

The emission characteristic can be properly changed by switching table data by an output from an I/O control unit; P13 serving as one of control inputs/outputs of the 15 system control unit mainly made up of the MPU; P11.

Reference symbols P8 denote image memories which are arranged for respective R, G, and B processing circuits and have addresses for the total number of display pixels of the panel (in this case, 240 horizontal * 240 vertical lines 20 * 3). Each memory stores luminance data each panel pixel should emit. Luminance data are dot-sequentially read out to display an image stored in the memory on the panel.

Luminance data is output from P8 under address control of the RAM controller; P12.

25 Data is written in P8 under the control of the system control unit mainly made up of the MPU; P11. For a simple

test pattern, the MPU; P11 calculates, generates, and writes luminance data to be stored at each address in P8. For a natural still image pattern, an image file stored in, e.g., an external computer is read via a serial

5 communication I/F; P16 serving as one of inputs/outputs of the system control unit mainly made up of the MPU; P11, and the read file is written in the image memory; P8.

Reference symbols P9 denote data selectors which determine whether image data to be output is data from the 10 image memory; P8 or data from the A/D unit; P6 (input video signal system), on the basis of an output from the I/O control unit; P13 serving as one of control inputs/outputs of the system control unit mainly made up of the MPU; P11.

In addition to the two input selection systems, a mode 15 of generating a fixed value from P9 is prepared. This mode can be selected by P13 to output the fixed value. In this mode, e.g., an adjustment signal such as a whole white pattern can be displayed at a high speed without any external input.

20 Reference symbols P10 denote horizontal 1-line memory means arranged for respective primary color signals. The horizontal 1-line memory means; P10 rearrange luminance data input parallel to the three, R, G, and B systems into an order corresponding to the color layout of the panel, 25 convert the luminance data into a serial signal of one system, and output the converted signal to an X driver via

a latch means; P22 in accordance with a control signal from a line memory control unit; P21.

The system control unit is mainly comprised of the MPU; P11, the serial communication I/F; P16, the I/O control unit; P13, the D/A unit; P14, the A/D unit; P15, a data memory; P17, and a user SW means; P18.

The system control unit receives a user request from the user SW means; P18 or serial communication I/F; P16, and outputs a corresponding control signal from the I/O control unit; P13 or D/A unit; P14 to meet the request.

In addition, the system control unit performs optimal automatic control by receiving a system monitoring signal from the A/D unit; P15 and outputting a corresponding control signal from the I/O control unit; P13 or D/A unit; P14.

This embodiment can realize generation of a test pattern, change of the tone level, and display control such as brightness or color control in accordance with a user request. By monitoring the average video level from the video detection unit; P4 by the A/D unit; P15, automatic control such as ABL can be achieved.

Since the data memory; P17 is adopted, it can store the user adjustment amount.

As shown in Fig. 3, the driver circuit comprises a Y-driver control timing generation unit P19 and an X-driver control timing generation unit P20. Both the Y-driver

control generation unit P19 and X-driver control timing generation unit P20 receive signals CLK1, CLK2, and SYNC2 to generate Y-driver control and X-driver control signals. Reference symbol P21 denotes a control unit for performing 5 timing control of the line memory; P10. P21 receives the signals CLK1, CLK2, and SYNC2, and generates R, G, and B_WRT control signals for writing luminance data in the line memory, and R, G, and B_RD control signals for reading out luminance data from the line memory in an order 10 corresponding to the color layout of the panel.

Fig. 5 is a timing chart showing the operation of the display panel driving apparatus described above. A signal T104 represents a color sample data string waveform obtained by displaying one of R, G, and B colors. The signal 15 T104 is made up of 240 data strings per horizontal period. These data strings are written in the line memory; P10 in one horizontal period in accordance with a control signal. In the next horizontal period, data strings are read out 20 from the line memory; P10 of each color at a frequency three times higher than the write frequency, thereby obtaining 720 luminance data strings per horizontal period, like T105.

An X & Y-driver timing generation unit P1001 receives a driver output control signal from the MPU; P11 and control 25 signals from the Y-driver control timing generation unit P19 and X-driver control timing generation unit, and

outputs signals necessary for the control of the X driver. The necessary signals are a shift clock serving as a PWM data shift control signal for reading luminance data from P22 into a shift register; P1101, a shift clock serving as 5 a correction data shift control signal for reading correction data from P1201 into a shift register; P1107, and ~LD/ST pulses functioning as a horizontal period trigger and PWM start trigger as a PWM control signal and D/A control signal to PWM generation units; P1102 and D/A 10 units; P1103 for fetching data read in the shift registers P1101 and P1107 in the internal memory means (not shown) of the PWM generation units; P1102 and D/A units; P1103.

The X & Y-driver timing generation unit P1001 outputs a PWM control signal for controlling the gate of the D/A 15 output of each PWM generator P1102, and a D/A control signal for controlling the gate of the D/A output of each D/A P1103. As far as the PWM control signal and D/A control signal is disabled, the PWM generator P1102 and D/A P1103 do not output any signals.

20 The X & Y-driver timing generation unit P1001 outputs correction table ROM control signal.

The X & Y-driver timing generation unit P1001 outputs a Yout control signal for controlling the gate of a portion of a pre-driver unit that outputs a signal to an FET means 25 in selecting a row wiring line. When the Yout control signal is disabled, all the row wiring lines keep receiving

a non-selection potential.

The shift register; P1101 reads the luminance data strings of 720 column wiring lines from the latch means; P22 every horizontal period in accordance with a shift clock 5 which synchronizes with luminance data such as T107 in Fig. 5 from the X & Y-driver timing generation unit P1001. Then, the shift register P1101 transfers 720 data of one horizontal line to the PWM generator units; P1102 at once in accordance with an "L"-level ~LD/ST pulse such as T108.

10 The shift register; P1107 reads the column wiring driving current data strings of 720 column wiring lines from the data selector means; P1201 every horizontal period in accordance with a shift clock, similar to luminance data. Then, the shift register P1107 transfers 720 data of one 15 horizontal line to the D/A units; P1103 at once in synchronism with an "L"-level ~LD/ST pulse such as T108.

When the X & Y-driver timing generation unit P1001 does not enable any PWM control signal to the PWM GEN P1102, the PWM generator P1102 does not output any signal. If the 20 PWM control signal is enabled, the PWM generator P1102 outputs a PWM output to a switching means; P1104. When the X & Y-driver timing generation unit P1001 does not enable any D/A control signal to the D/A P1103, the D/A unit P1103 does not output any current. If the D/A control signal is 25 enabled, the D/A P1103 outputs a current output to the switching means; P1104.

A correction table ROM; P1202 is a memory means for storing, for R, G, and B, data of a current amplitude value to be flowed through 720*240 surface-conduction type devices of the display panel; P2000. The correction table 5 ROM P1202 undergoes read address control in accordance with an correction table ROM control signal from the X & Y-driver timing generation unit P1001, and outputs data of 720 current amplitude values for one row to be scanned, such as T105 shown in Fig. 5, every horizontal period.

10 A current value for driving the column wiring line (i.e., surface-conduction type devices) is optimized using the correction table ROM; P1202 for each device, thereby making the luminance uniform.

15 The data selector means; P1201 is adopted for a case in which the correction table ROM; P1202 is not used in order to reduce the cost or the like. The data selector means; P1201 outputs, to the shift register; P1107 in accordance with a switching signal from the I/O control unit; P13, correction setting data output from the I/O control unit; 20 P13 serving as one of control inputs/outputs of the system control unit mainly made up of the MPU; P11.

This circuit controls correction data with a current amplitude, but may control it with a voltage amplitude.

25 The PWM generator unit; P1102 arranged on each column wiring line receives luminance data from the shift register; P1101 when the ~LD/ST pulse T108 in Fig. 5 is at

"L" level. After the ~LD/ST pulse rises, the PWM generator unit P1102 generates a pulse signal having a pulse width proportional to the data size every horizontal period, such as a waveform T110 in Fig. 5.

5 The D/A unit; P1103 arranged on each column wiring line is a digital-to-analog converter for a current output. This D/A unit P1103 receives data of a current amplitude value from the shift register; P1107, and generates a driving current having a current amplitude proportional to 10 the data size every horizontal period, such as a waveform T111 in Fig. 5.

Reference symbols P1104 denote the switching means each formed from a transistor and the like. Each P1104 applies a current output from the D/A unit; P1103 to a column 15 wiring line while an output from the PWM generation unit; P1102 is valid, and grounds the column wiring line while an output from the PWM generation unit; P1102 is invalid. A column wiring driving waveform is represented by T111 of Fig. 5.

20 Diode means; P1105 arranged on respective column wiring lines are connected on the common side to a Vmax regulator; P1106. The Vmax regulator; P1106 is a constant-voltage source capable of sucking a current, and forms together with the diode means; P1105 a protection 25 circuit for preventing an excessive voltage from being applied to 720*240 surface-conduction type devices of the

display panel; P2000.

The protection voltage (potential defined by Vmax and -Vss applied in scanning and selection of a row wiring line) is applied by the D/A unit; P14 serving as one of control 5 inputs/outputs of the system control unit mainly made up of the MPU; P11.

Hence, the Vmax regulator P1106 can change the potential Vmax (or potential -Vss) in order to control the luminance in addition to avoid an excessive voltage to the 10 device.

A Y shift register receives from the X & Y-driver timing generation unit P1001 a shift clock of a horizontal period and a trigger signal of a vertical period for supplying a row scanning start trigger, and sequentially 15 outputs selection signals for scanning row wiring lines to pre-driver units arranged on respective row wiring lines.

When the X & Y-driver timing generation unit P1001 inputs an OFF signal to each pre-driver unit, the gate of a portion which outputs a signal to the FET means is turned off, and all the devices keep receiving a non-selection 20 potential. When the X & Y-driver timing generation unit P1001 inputs an ON signal to the pre-driver unit, the gate of the portion which outputs a signal to the FET means is turned on, and row selection starts.

25 The output unit for driving each row wiring line is made up of, e.g., a transistor means, FET means, and diode

means. The pre-driver drives this output terminal at a high response speed, and functions as a circuit for controlling application of a scanning signal. The pre-driver unit comprises a gate circuit for controlling an output to the 5 FET means. In selecting a row, the FET means applies the potential $-V_{ss}$ from a constant-voltage regulator unit to the row wiring line via a switching means which is turned on in selection. In non-selection, the transistor means applies a potential V_{uso} from the constant-voltage 10 regulator unit to the row wiring line via the switching means which is turned on when no row is selected. T112 shown in Fig. 5 is an example of a row wiring driving waveform.

Fig. 6 is a block diagram showing the power source line layout of the above-described image display apparatus. 15 As shown in Fig. 6, a power source for the video/control circuit supplies power to the control circuit P11 and video circuit via a line L1. As described above, the video circuit sends a control signal to the X & Y-driver timing generation circuit P1001, and sends image data to the latch 20 means P22 on the basis of an image signal input (Video In). A power source for the driver circuit supplies power to the modulation circuit via a line L2. As described above, the modulation circuit receives an output from the X & Y-driver timing generation circuit P1001, an output from the latch 25 means P22, and an output from the data selector P1201, and parallel-outputs data in the column direction of the

display panel P2000. A high-voltage power source supplies a high voltage V_a to the display panel P2000 via a line L3. An auxiliary power source such as a capacitor or battery supplies power to the control circuit P11 and video circuit 5 via a line L4. A power source circuit P24 is connected to a power source monitoring circuit P25.

Fig. 7 is a block diagram showing the flow of a control signal for controlling supply of power to the above-described image display apparatus. As shown in 10 Fig. 7, the control circuit P11 controls the video circuit, power source circuit, scanning circuit, and modulation circuit.

Fig. 8 is a circuit diagram showing the power source circuit P24 and power source monitoring circuit P25. 15 The circuit shown in Fig. 8 gives the power source circuit P24 an emergency shutdown function, and includes the power source P24 for converting external AC power to DC power necessary for each circuit, the power monitoring circuit P25 for measuring the voltage of the power source P24 and when the voltage exceeds a specified potential, outputting a power source reset signal to the MPU; P11, and an auxiliary power source P26 for supplying power to each circuit while the following emergency shutdown sequence is completed when the power source is turned off. 20 The auxiliary power source P26 may be formed from a capacitor or battery. The power source monitoring circuit 25

P25 is a resistor which is designed to divide a voltage into 5 V as a typical value. The power source monitoring circuit P25 is set to output a power reset signal to the MPU; P11 when the voltage becomes 3.5 V or less or 6 V or more.

5 The constant-voltage regulator unit (not shown) for generating the potentials -Vss and Vuso is controlled by the D/A unit; P14 serving as one of control inputs/outputs of the system control unit mainly made up of the MPU; P11.

10 The high-voltage power source unit (not shown) is also controlled by the D/A unit; P14 as one of control inputs/outputs of the system control unit mainly made up of the MPU; P11.

15 The potential Vuso may be 0 V. In this case, the constant-voltage regulator unit for generating the potential Vuso can be replaced with a GND circuit.

The power-on sequence of this embodiment will be explained with reference to the flow chart of Fig. 9.

20 In step S1, if a power switch as one of the user SW means; P18 is turned on, the power sources of respective circuits are turned on to activate these circuits in step S2.

25 In step S3, immediately after the power source is turned on, a PWM control signal output from the X & Y-driver timing generation unit P1001 to the PWM generator is kept disabled. The gate is kept off for an output from the PWM generator P1102, and no PWM signal is applied to the panel.

Upon power-on operation, data in the shift register is not determined, but no driving signal is applied to the surface-conduction type device; P2001 of the display panel P2000, thereby preventing degradation and destruction of 5 the device caused by an indeterminate signal upon power-on operation.

If the system control unit is activated in step S2, the MPU; P11 of the system control unit starts counting vertical sync signals of an image in step S5. Data in the 10 shift register is not determined immediately upon power-on operation, and the MPU; P11 counts vertical sync signals until data in the shift register stabilizes. In this case, the shift register satisfactorily stabilizes when the count value reaches three. That is, when the count value reaches 15 three, and the shift register stabilizes, control of the PWM generator P1102 starts in step S6. In step S7, the X & Y-driver timing generation unit P1001 outputs an ON signal as a PWM control signal to the PWM generator P1102 to turn on the gate of the PWM generator. Then, a PWM output is 20 applied to the surface-conduction type device; P2001 of the display panel P2000 via the switching means; P1104.

If the count value reaches three, and the shift register stabilizes in step S5, the MPU; P11 inputs to the high-voltage power source unit; P30 via the D/A unit; P14 25 a signal for controlling a high-voltage potential from 0 V to a set value (in this case, 5 to 10 kV) in step S8. In

step S9, an output from the high-voltage power source unit; P30 changes to the set value (in this case, 5 to 10 kV).

When the power switch is turned on, each signal is applied by this sequence without degrading or damaging the 5 device by an indeterminate signal to the surface-conduction type device; P2001 of the display panel; P2000.

In this embodiment, a time within which data in the shift register stabilizes is measured in advance, vertical sync signals are counted, and when the count value reaches 10 three, the next sequence is executed. The delay time depends on the time within which data in the shift register stabilizes, and is not necessarily limited by this time. Although the delay time is calculated based on vertical sync signals in this embodiment, the delay time may be calculated 15 based on horizontal sync signals or a delay timer may be attached. The delay method is not limited. Further, in this embodiment, an output from the driving circuit unit is controlled by outputting a gate signal from the X & Y-driver timing generation unit P1001. However, the 20 output control is not limited to this, and the MPU; P11 of the system control unit or another control system may be used.

Moreover, the power source can be turned on by the same sequence even in a circuit arrangement in which the 25 amplitude of luminance data is modulated to PWM-output correction data, instead of PWM-outputting luminance data

in step S7.

[Second Embodiment]

This embodiment adopts a different power-on sequence with the same arrangement as in the first embodiment. The 5 power-on sequence in the second embodiment will be explained with reference to the flow chart of Fig. 10.

If a power switch as one of user SW means; P18 is turned on (step S11), the power sources of respective circuits are turned on to activate these circuits (step S12).

10 Immediately after the power source is turned on, a D/A control signal output from an X & Y-driver timing generation unit P1001 to a D/A unit P1003 is kept disabled (step S3). The gate is kept off for an output from the D/A unit P1103, and no set current value corresponding to correction data 15 is applied to the panel. Upon power-on operation, data in a shift register is not determined, but no driving signal is applied to a surface-conduction type device; P2001 of a display panel; P2000, thereby preventing degradation and destruction of the device caused by an indeterminate signal 20 upon power-on operation.

If a system control unit is activated (step S12), an MPU; P11 of the system control unit starts counting vertical sync signals of an image. Data in the shift register is not determined immediately upon power-on operation, and the 25 MPU; P11 counts vertical sync signals until data in the shift register stabilizes. In this case, the shift

register satisfactorily stabilizes when the count value reaches three.

That is, when the count value reaches three, and the shift register stabilizes (step S15), the X & Y-driver 5 timing generation unit P1001 outputs an ON signal as a D/A control signal to the D/A unit P1103 (step S16) to turn on the gate of the D/A unit; P1103. Then, a set current value is applied to the surface-conduction type device; P2001 of the display panel; P2000 via a switching means; P1104.

10 If the count value reaches three, and the shift register stabilizes (step S15), the MPU; P11 inputs to a high-voltage power source unit; P30 via a D/A unit P14 a signal for controlling a high-voltage potential from 0 V to a set value (in this case, 5 to 10 kV) (step S18). Then, 15 an output from the high-voltage power source unit; P30 changes to the set value (in this case, 5 to 10 kV) (step S19).

When the power switch is turned on, each signal is applied by this sequence without degrading or damaging the 20 device by an indeterminate signal to the surface-conduction type device; P2001 of the display panel P2000.

In this embodiment, a time within which data in the shift register stabilizes is measured in advance, vertical sync signals are counted, and when the count value reaches 25 three, the next sequence is executed. The delay time depends on the time within which data in the shift register

stabilizes, and is not necessarily limited by this time. Although the delay time is calculated based on vertical sync signals in this embodiment, the delay time may be calculated based on horizontal sync signals or a delay timer may be
5 attached. The delay method is not limited. Further, in this embodiment, an output from the driving circuit unit is controlled by outputting a gate signal from the X & Y-driver timing generation unit P1001. However, the output control is not limited to this, and the MPU; P11 of
10 the system control unit or another control system may be used.

Moreover, the power source can be turned on by the same sequence even in a circuit arrangement in which the amplitude of luminance data is modulated to PWM-output
15 correction data, instead of D/A-outputting a correction value in step S17.

[Third Embodiment]

This embodiment employs a different power-on sequence with the same arrangement as in the first
20 embodiment. The power-on sequence in the third embodiment will be explained with reference to Fig. 11.

1)

If a power switch as one of user SW means; P18 is turned on (step S21), the power sources of respective circuits are
25 turned on to activate these circuits (step S22).

Immediately after the power source is turned on, a PWM

control signal output from an X & Y-driver timing generation unit P1001 to a PWM generator P1102, and a D/A control signal output from the X & Y-driver timing generation unit P1001 to a D/A unit P1003 are kept disabled (step S23). The gate 5 is kept off for an output from the PWM generator P1102, and no PWM signal is applied to a panel. The gate is kept off for an output from the D/A unit P1103, and no set current value corresponding to correction data is applied. Upon power-on operation, data in a shift register is not 10 determined, but no driving signal is applied to a surface-conduction type device; P2001 of a display panel; P2000, thereby preventing degradation and destruction of the device caused by an indeterminate signal upon power-on operation.

15 If a system control unit is activated (step S22), an MPU; P11 of the system control unit starts counting vertical sync signals of an image. Data in the shift register is not determined immediately upon power-on operation, and the MPU; P11 counts vertical sync signals until data in the 20 shift register stabilizes. In this case, the shift register satisfactorily stabilizes when the count value reaches three.

That is, when the count value reaches three, and the shift register stabilizes (step S25), the X & Y-driver 25 timing generation unit P1001 outputs an ON signal as a PWM control signal to the PWM generator P1102. At the same time,

the X & Y-driver timing generation unit P1001 outputs an ON signal as a D/A control signal to the D/A unit P1103 (step S26). Then, the gate of the PWM generator is turned on, and the gate of the D/A unit; P1103 is turned on. A PWM output and set current value are applied to the surface-conduction type device; P2001 of the display panel; P2000 via a switching means; P1104.

If the count value reaches three, and the shift register stabilizes (step S25), the MPU; P11 inputs to a high-voltage power source unit; P30 via a D/A unit P14 a signal for controlling a high-voltage potential from 0 V to a set value (in this case, 5 to 10 kV) (step S28). Then, an output from the high-voltage power source unit; P30 changes to the set value (in this case, 5 to 10 kV) (step S29).

When the power switch is turned on, each signal is applied by this sequence without degrading or damaging the device by an indeterminate signal to the surface-conduction type device; P2001 of the display panel; P2000.

In this embodiment, a time within which data in the shift register stabilizes is measured in advance, vertical sync signals are counted, and when the count value reaches three, the next sequence is executed. The delay time depends on the time within which data in the shift register stabilizes, and is not necessarily limited by this time. Although the delay time is calculated based on vertical sync

signals in this embodiment, the delay time may be calculated based on horizontal sync signals or a delay timer may be attached. The delay method is not limited. Further, in this embodiment, an output from the driving circuit unit 5 is controlled by outputting a gate signal from the X & Y-driver timing generation unit P1001. However, the output control is not limited to this, and the MPU; P11 of the system control unit or another control system may be used.

10 The power source can be turned on by the same sequence even in a circuit arrangement in which the amplitude of luminance data is modulated to PWM-output correction data, instead of D/A-outputting a correction value in step S27.

[Fourth Embodiment]

15 This embodiment relates to a different power-on sequence with the same arrangement as in the first embodiment. The power-on sequence in the fourth embodiment will be explained with reference to Fig. 12.

1) If a power switch as one of user SW means; P18 is turned 20 on (step S31), the power sources of respective circuits are turned on to activate these circuits (step S32).

Immediately after the power source is turned on, a Yout control signal output from an X & Y-driver timing generation unit P1001 to a pre-driver is kept disabled (step S33). The 25 gate is kept off for an output from the pre-driver to an FET means, the row wiring side is kept unselected, and no

selection voltage is applied to a panel. Upon power-on operation, data in a shift register is not determined, but no selection potential in scanning is applied to a surface-conduction type device; P2001 of a display panel; 5 P2000, thereby preventing degradation and destruction of the device caused by an indeterminate signal upon power-on operation.

If a system control unit is activated (step S32), an MPU; P11 of the system control unit starts counting vertical 10 sync signals of an image. Data in the shift register is not determined immediately upon power-on operation, and the MPU; P11 counts vertical sync signals until data in the shift register stabilizes. In this case, the shift register satisfactorily stabilizes when the count value 15 reaches three.

That is, when the count value reaches three, and the shift register stabilizes (step S35), the X & Y-driver timing generation unit P1001 outputs an ON signal as a Yout control signal to the pre-driver (step S36). Then, the gate 20 of a portion which outputs a signal to the FET means is turned on to start row selection.

If the count value reaches three, and the shift register stabilizes (step S35), the MPU; P11 inputs to a high-voltage power source unit; P30 via a D/A unit P14 a 25 signal for controlling a high-voltage potential from 0 V to a set value (in this case, 5 to 10 kV) (step S38). Then,

an output from the high-voltage power source unit; P30 changes to the set value (in this case, 5 to 10 kV) (step S39).

When the power switch is turned on, each signal is applied by this sequence without degrading or damaging the device by an indeterminate signal to the surface-conduction type device; P2001 of the display panel; P2000.

In this embodiment, a time within which data in the shift register stabilizes is measured in advance, vertical sync signals are counted, and when the count value reaches three, the next sequence is executed. The delay time depends on the time within which data in the shift register stabilizes, and is not necessarily limited by this time. Although the delay time is calculated based on vertical sync signals in this embodiment, the delay time may be calculated based on horizontal sync signals or a delay timer may be attached. The delay method is not limited. Further, in this embodiment, an output from the driving circuit unit is controlled by outputting a gate signal from the X & Y-driver timing generation unit P1001. However, the output control is not limited to this, and the MPU; P11 of the system control unit or another control system may be used.

The power source can be turned on by the same sequence even in a circuit arrangement in which the amplitude of luminance data is modulated to PWM-output correction data,

instead of a Y output in step S37.

Upon power-on operation, the modulation signal side in the first to third embodiments, or the scanning signal side in the fourth embodiment stops an output for 5 stabilizing data in the shift register. Alternatively, both the modulation signal side and scanning signal side may be stopped.

[Fifth Embodiment]

This embodiment concerns a different power-on 10 sequence with the same arrangement as in the first embodiment. This embodiment will describe a sequence of stopping either one of an output from a scanning circuit and an output from a modulation circuit until the power source voltages of the scanning circuit and modulation 15 circuit reach desired values upon power-on operation. The power-on sequence in the fifth embodiment will be explained with reference to Fig. 13.

If a power switch as one of user SW means; P18 is turned on (step S41), the power sources of respective circuits are 20 turned on to activate these circuits (step S42). Immediately after the power source is turned on, a PWM control signal output from an X & Y-driver timing generation unit P1001 to a PWM generator P1102 is kept disabled (step S43). The gate is kept off for an output from the PWM 25 generator P1102, and no PWM signal is applied to a panel.

Upon power-on operation, the power source voltage

the row wiring line; P2002 side and the power source voltage (output voltage from the Vmax regulator; P1106) of the modulation circuit on the column wiring line; P2003 side reach desired values (step S45), the X & Y-driver timing 5 generation unit P1001 outputs an ON signal as a PWM control signal to the PWM generator P1102 (step S46). Then, the gate of the PWM generator is turned on to apply a PWM output to the surface-conduction type device; P2001 of the display panel P2000 via a switching means; 1104.

10 If the count value reaches three, and the power source voltage (output voltages from the Vuso regulator and -Vss regulator) of the scanning circuit on the row wiring line; P2002 side and the power source voltage (output voltage from the Vmax regulator; P1106) of the modulation circuit on the 15 column wiring line; P2003 side reach desired values (step S45), the MPU; P11 inputs to a high-voltage power source unit; P30 via a D/A unit P14 a signal for controlling a high-voltage potential from 0 V to a set value (in this case, 5 to 10 kV) (step S48). Then, an output from the 20 high-voltage power source unit; P30 changes to the set value (in this case, 5 to 10 kV) (step S49).

When the power switch is turned on, each signal is applied by this sequence without degrading or damaging the device by an indeterminate power source voltage to the 25 surface-conduction type device; P2001 of the display panel P2000.

(output voltages from a Vuso regulator and -Vss regulator) of the scanning circuit on a row wiring line; P2002 side, and the power source voltage (output voltage from a Vmax regulator; P1106) of the modulation circuit on a column wiring line; P2003 side do not reach desired values.

However, no driving signal is applied to a surface-conduction type device; P2001 of a display panel; P2000, thereby preventing degradation and destruction of the device caused by an indeterminate power source voltage upon power-on operation.

If a system control unit is activated (step S42), an MPU; P11 of the system control unit starts counting vertical sync signals of an image. The power source voltage (output voltages from the Vuso regulator and -Vss regulator) of the scanning circuit on the row wiring line; P2002 side, and the power source voltage (output voltage from the Vmax regulator; P1106) of the modulation circuit on the column wiring line; P2003 side do not reach desired values. The MPU; P11 counts vertical sync signals until the power source voltages of the scanning circuit and modulation circuit reach desired values. In this case, the power source voltages of the scanning circuit and modulation circuit reach desired values when the count value reaches three.

That is, when the count value reaches three, and the power source voltage (output voltages from the Vuso regulator and -Vss regulator) of the scanning circuit on

In this embodiment, the gate of the PWM output unit; P1102 is controlled to be kept off until the power source voltage (output voltages from the Vuso regulator and -Vss regulator) of the scanning circuit on the row wiring line; 5 P2002 side and the power source voltage (output voltage from the Vmax regulator; P1106) of the modulation circuit on the column wiring line; P2003 side reach desired values. Alternatively, the gate of the PWM output unit; P1102 may be controlled by turning off the gate of a D/A unit; P1103 10 for controlling the current amplitude, or by turning off the gate of a pre-driver on the row wiring line; P2002 side.

In this embodiment, a time is measured in advance within which the power source voltage (output voltages from the Vuso regulator and -Vss regulator) of the scanning circuit on the row wiring line; P2002 side and the power source voltage (output voltage from the Vmax regulator; P1106) of the modulation circuit on the column wiring line; 15 P2003 side reach desired values. Then, vertical sync signals are counted, and when the count value reaches three, 20 the next sequence is executed. The delay time depends on the time within which the power source voltage (output voltages from the Vuso regulator and -Vss regulator) of the scanning circuit on the row wiring line; P2002 side and the power source voltage (output voltage from the Vmax 25 regulator; P1106) of the modulation circuit on the column wiring line; P2003 side reach desired values. The delay

time is not necessarily limited by this time. Although the delay time is calculated based on vertical sync signals in this embodiment, the delay time may be calculated based on horizontal sync signals or a delay timer may be attached.

5 The delay method is not limited to a specific one. Further, in this embodiment, an output from the driving circuit unit is controlled by outputting a gate signal from the X & Y-driver timing generation unit P1001. However, the output control is not limited to this, and the MPU; P11 of 10 the system control unit or another control system may be used.

The power source can be turned on by the same sequence even in a circuit arrangement in which the amplitude of luminance data is modulated to PWM-output correction data,

15 instead of PWM-outputting luminance data in step s47.

[Sixth Embodiment]

This embodiment relates to a power-off sequence with the same arrangement as in the first embodiment. The power-off sequence in the sixth embodiment will be 20 explained with reference to Fig. 14.

If a power switch as one of user SW means; P18 is turned off (step S51), a power stop signal is input to an MPU; P11 via an I/O control unit; P13 (step S52).

If the power source stop signal is input to the MPU; 25 P11, the MPU; P11 outputs a stop signal for a driver output control signal to an X & Y-driver timing generation unit

P1001. The X & Y-driver timing generation unit P1001 immediately outputs a signal for turning off the gate of a PWM generator; P1102 (step S53).

This gate-off signal immediately stops a PWM output 5 (step S54). In this state, no driving signal is applied to a surface-conduction type device; P2001 of a display panel; P2000. The surface-conduction type device; P2001 of the display panel; P2000 is not deteriorated or destructed regardless of unstable voltages output upon 10 power-off operation from the power source voltage (output voltages from a Vuso regulator and -Vss regulator) of a scanning circuit on a row wiring line; P2002 side and the power source voltage (output voltage from a Vmax regulator; P1106) of a modulation circuit on a column wiring line; 15 P2003.

After the X & Y-driver timing generation unit P1001 outputs the signal for turning off the gate of the PWM generator; P1102 (step S53), supply of power to a driving circuit unit and video circuit unit is stopped (step S55), 20 and supply of power to a system control unit is stopped (step S56).

When the power switch is turned off, supply of power is stopped by this sequence without degrading or damaging the device by an indeterminate power source voltage to the 25 surface-conduction type device; P2001 of the display panel P2000.

In this embodiment, when the power source is turned off, the gate of the PWM output unit; P1102 is controlled to be immediately turned off. Alternatively, the gate of the PWM output unit P1102 may be controlled by turning off 5 the gate of a D/A unit; P1103 for controlling the current amplitude, or by turning off the gate of a pre-driver on the row wiring line; P2002 side.

In this embodiment, an output from the driving circuit unit is controlled by outputting a gate signal from 10 the X & Y-driver timing generation unit P1001. However, the output control is not limited to this, and the MPU; P11 of the system control unit or another control system may be used.

The power source can be turned off by the same sequence 15 even in a circuit arrangement in which the amplitude of luminance data is modulated to PWM-output correction data.

[Seventh Embodiment]

This embodiment concerns a sequence in emergency shutdown of the power source when an outlet is removed or 20 power fails, with the same arrangement as in the first embodiment. To emergently shutting down a power source when an outlet is removed or power fails, an emergency shutdown circuit as shown in Fig. 8 is required. The power shutdown sequence in the seventh embodiment will be 25 explained with reference to Fig. 15.

If an outlet is removed or power fails (step S61),

a power source monitoring circuit; P25 observes a voltage abnormality (step S62). The power source monitoring circuit; P25 outputs a power source reset signal to an MPU; P11 (step S63).

5 If the power source monitoring circuit; P25 inputs the power source reset signal to the MPU; P11, the MPU; P11 outputs a stop signal for a driver output control signal to an X & Y-driver timing generation unit P1001. The X & Y-driver timing generation unit P1001 immediately outputs
10 a signal for turning off the gate of a PWM generator; P1102 (step S64).

This gate-off signal immediately stops a PWM output (step S65). In this state, no driving signal is applied to a surface-conduction type device; P2001 of a display panel; P2000. The surface-conduction type device; P2001 of the display panel; P2000 is not deteriorated or destructed regardless of unstable voltages output upon power-off operation from the power source voltage (output voltages from a Vuso regulator and -Vss regulator) of a
15 scanning circuit on a row wiring line; P2002 side and the power source voltage (output voltage from a Vmax regulator; P1106) of a modulation circuit on a column wiring line; P2003.

After the X & Y-driver timing generation unit P1001
25 outputs the signal for turning off the gate of the PWM generator; P1102 (step S64), supply of power to all circuits

is stopped (step S67).

While at least step S65 is completed in this sequence, an auxiliary power source; P26 keeps supplying power.

When the power switch is emergently shut down, supply 5 of power is stopped by this sequence without degrading or damaging the device by an indeterminate power source voltage to the surface-conduction type device; P2001 of the display panel; P2000.

In this embodiment, when the power source is turned 10 off, the gate of the PWM output unit; P1102 is controlled to be immediately turned off. Alternatively, the gate of the PWM output unit P1102 may be controlled by turning off the gate of a D/A unit; P1103 for controlling the current amplitude, or by turning off the gate of a pre-driver on 15 the row wiring line; P2002 side.

In this embodiment, an output from the driving circuit unit is controlled by outputting a gate signal from the X & Y-driver timing generation unit P1001. However, the output control is not limited to this, and the MPU; P11 20 of the system control unit or another control system may be used.

The power source can be turned off by the same sequence even in a circuit arrangement in which the amplitude of luminance data is modulated to PWM-output correction data.

25 The image display apparatus control method of the present invention has been described. An image display

apparatus will be explained.

(Arrangement and Manufacturing Method of Display Panel)

The arrangement and manufacturing method of the 5 display panel of an image display apparatus to which the present invention is applied will be exemplified.

Fig. 16 is a perspective view of the display panel used in this embodiment in which part of the panel is cut away in order to show the internal structure. In Fig. 16, 10 reference numeral 1005 denotes a rear plate; 1006, a side wall; and 1007, a face plate. The rear plate 1005 to face plate 1007 constitute an airtight container for keeping the interior of the display panel vacuum. In assembling the airtight container, it is necessary to seal the container 15 in order to make the joint portions of the respective members hold a sufficient strength and airtight condition. For example, frit glass is applied to joint portions, and baked in the outer air or a nitrogen atmosphere at 400 to 500°C for 10 min or more, thereby sealing the container. 20 A method for evacuating the airtight container will be described later.

A substrate 1001 is fixed to the rear plate 1005, and $n \times m$ cold cathode devices 1002 are formed on the substrate. (n and m are positive integers equal to 2 or more, and are 25 properly set in accordance with a target number of display pixels. For example, in a display apparatus for

high-resolution television display, $n = 3,000$ or more, and $m = 1,000$ or more are preferable. In this embodiment, $n = 3,072$ or more, and $m = 1,024$.) The $n \times m$ cold cathode devices are arranged in a simple matrix with m row-direction wiring lines 1003 and n column-direction wiring lines 1004. The portion constituted by the substrate 1001 to column-direction wiring lines 1004 is called a multi electron beam source. The manufacturing method and structure of the multi electron beam source will be described in detail later.

In Fig. 16, the substrate 1001 of the multi electron beam source is fixed to the rear plate 1005 of the airtight container. If, however, the substrate 1001 of the multi electron beam source has a sufficient strength, the substrate 1001 of the multi electron beam source may be used as the rear plate of the airtight container.

A fluorescent film 1008 is formed on the lower surface of the face plate 1007. To display a color image by the fluorescent film 1008, the fluorescent film 1008 is coated with three, red, green, and blue primary color fluorescent substances used in the CRT field. As shown in Fig. 17(a), fluorescent substances of the respective colors are applied in stripes, and black conductive members 1010 are provided between the stripes of the fluorescent substances. The purpose of providing the black conductive members 1010 is to prevent display color misregistration even if the

electron-beam irradiation position is shifted to some extent, to prevent a decrease in display contrast by shutting off reflection of external light, and to prevent charge-up of the fluorescent film by an electron beam. The 5 black conductive members 1010 is mainly made of graphite, but may be made of another material as far as the material meets the purpose.

Fluorescent substances of the three primary colors are not limited to a striped layout shown in Fig. 17(a). 10 For example, fluorescent substances may adopt a delta layout as shown in Fig. 17(b) or another layout.

In fabricating a monochrome display panel, a fluorescent substance material of a single color may be used for the fluorescent film 1008, and the black conductive 15 member need not always be used.

A metal back 1009, which is well-known in the CRT field, is formed on a surface of the fluorescent film 1008 on the rear plate side. The purpose of forming the metal back 1009 is to improve the light utilization ratio by 20 mirror-reflecting part of light emitted by the fluorescent film 1008, to protect the fluorescent film 1008 from collision with negative ions, to use the metal back 1009 as an electrode for applying an electron beam acceleration voltage, and to use the metal back 1009 as the conductive 25 path of electrons which have excited the fluorescent film 1008. The metal back 1009 is formed by forming the

fluorescent film 1008 on the face plate substrate 1007, smoothing the surface of the fluorescent film, and depositing Al on the smoothed surface by vacuum evaporation. If a low-voltage fluorescent substance material is used for the fluorescent film 1008, the metal back 1009 is not used.

To apply an acceleration voltage or improve the conductivity of the fluorescent film, transparent electrodes made of, e.g., ITO may be provided between the face plate substrate 1007 and the fluorescent film 1008.

Reference symbols Dx1 to Dx_m, Dy1 to Dyn, and Hv denote electric connection terminals for the airtight structure that are provided to electrically connect the display panel and an electric circuit (not shown). Dx1 to Dx_m are electrically connected to the row-direction wiring lines 1003 of the multi electron beam source; Dy1 to Dyn, to the column-direction wiring lines 1004 of the multi electron beam source; and Hv, to the metal back 1009 of the face plate.

To evacuate the interior of the airtight container, an exhaust pipe and vacuum pump (neither is shown) are connected after the airtight container is assembled, and then the interior of the airtight container is evacuated to a vacuum degree of about 10^{-7} [Torr]. Thereafter, the exhaust pipe is sealed. To maintain the vacuum degree in the airtight container, a getter film (not shown) is formed at a predetermined position in the airtight container immediately before/after sealing. The getter film is a

film formed by heating and evaporating a getter material mainly consisting of, e.g., Ba, by a heater or radio-frequency heating. The absorption effect of the getter film maintains a vacuum degree of 1×10^{-5} to 1×10^{-7} [Torr] 5 in the airtight container.

(Manufacturing Method of Multi Electron Beam Source)

A method of manufacturing the multi electron beam source used in the display panel of this embodiment will be described. In the multi electron beam source used in 10 the image display apparatus of the present invention, the material, shape, and manufacturing method of the cold cathode device are not particularly limited as long as an electron source is constituted by wiring cold cathode devices in a simple matrix. For example, cold cathode 15 devices such as surface-conduction type emitting devices, FE type emitting devices, or MIM type emitting devices can be used.

Under circumstances where low-cost display apparatuses having large display screens are required, the 20 surface-conduction type emitting device is especially preferable among these cold cathode devices. More specifically, the FE type device requires a high-precision manufacturing technique because the relative positions and shapes of the emitter cone and gate electrode greatly 25 influence electron emission characteristics. This is disadvantageous in attaining a large area and low

manufacturing cost. In the MIM type device, the insulating layer and upper electrode must be made thin and uniform. This is also disadvantageous in attaining a large area and low manufacturing cost.

5 In contrast to this, the surface-conduction type emitting device can be manufactured by a relatively simple method, and can achieve a large area and low manufacturing cost. The present inventors have also found that among the surface-conduction type emitting devices, a device having
10 an electron-emitting portion or its peripheral portion made of a fine particle film exhibits excellent electron emission characteristics and can be easily manufactured. Such device is most preferably used in the multi electron beam source of a high-luminance, large-screen image display
15 apparatus.

The basic arrangement, manufacture, and characteristics of a surface-conduction type emitting device preferable to the present invention will be described. After that, the structure of the multi electron beam source having many devices wired in a simple matrix will be described later. Note that the image display apparatus using the surface-conduction type emitting device will be called an SED (Surface conduction electron Emitter Display).

25 (Preferred Device Structure and Manufacturing Method
of Surface-Conduction Type Emitting

Device)

Typical arrangements of surface-conduction type emitting devices each having an electron-emitting portion or its peripheral portion made of a fine particle film 5 include two types of devices, namely flat and stepped type devices.

(Flat Surface-Conduction Type Emitting Device)

The device structure and manufacturing method of a 10 flat surface-conduction type emitting device will be described.

Figs. 18(a) and 18(b) are a plan view and a sectional view, respectively, for explaining the arrangement of the flat surface-conduction type emitting device. Referring 15 to Fig. 18, reference numeral 1101 denotes a substrate; 1102 and 1103, device electrodes; 1104, a conductive thin film; 1105, an electron-emitting portion formed by electrification forming processing; and 1113, a thin film formed by electrification activation processing.

As the substrate 1101, various glass substrates of 20 quartz glass, soda-lime glass, and the like, various ceramic substrates of alumina and the like, or any of those substrates with an insulating layer formed thereon can be employed.

The device electrodes 1102 and 1103 which are formed 25 on the substrate 1101 in parallel with the substrate surface

so as to face each other are made of a conductive material. Examples of the material are metals such as Ni, Cr, Au, Mo, W, Pt, Ti, Cu, Pd, and Ag, alloys of these metals, metal oxides such as $In_2O_3-SnO_2$, and semiconductors such as 5 polysilicon. These electrodes can be easily formed by a combination of a film formation technique such as vacuum evaporation and a patterning technique such as photolithography or etching. Another method (e.g., printing technique) may be used.

10 The shape of the device electrodes 1102 and 1103 is appropriately designed in accordance with the application purpose of the electron-emitting device. In general, an interval L between the electrodes is designed by selecting an appropriate value in a range of several hundred Å to 15 several hundred μm . The most preferable range applied to a display apparatus is from several μm to several ten μm . As for a thickness d of the device electrode, an appropriate value is selected in a range of several hundred Å to several μm .

20 The conductive thin film 1104 is formed from a fine particle film. The fine particle film is a film that contains a lot of fine particles (including islands like masses of particles) as film-constituting members. In microscopic view, individual fine particles exist to be 25 apart from each other, to be adjacent to each other, or to overlap each other.

A fine particle used for the fine particle film has a diameter falling within a range of several Å to several thousand Å, and preferably a range of 10 Å to 200 Å. The thickness of the fine particle film is properly set in 5 consideration of the following conditions. That is, conditions necessary for electrically connecting the device electrode 1102 or 1103, conditions necessary for performing electrification forming (to be described later), and conditions necessary for setting the electrical 10 resistance of the fine particle film to an appropriate value (to be described later). More specifically, the film thickness is set within a range of several Å to several thousand Å, and preferably a range of 10 Å to 500 Å.

Examples of a material used for forming the fine 15 particle film are metals such as Pd, Pt, Ru, Ag, Au, Ti, In, Cr, Fe, Zn, Sn, Ta, W, and Pb, oxides such as PdO, SnO₂, In₂O₃, PbO, and Sb₂O₃, borides such as HfB₂, ZrB₂, LaB₆, CeB₆, YB₄ and GdB₄, carbides such as TiC, ZrC, HfC, TaC, SiC, and WC, nitrides such as TiN, ZrN, and HfN, semiconductors 20 such as Si and Ge, and carbons. The material is appropriately selected from them.

As described above, the conductive thin film 1104 is formed from a fine particle film, and its sheet resistance is set to reside within a range of 10³ to 10⁷ (Ω/sq).

25 The conductive thin film 1104 and the device electrodes 1102 and 1103 partially overlap each other

because they are desirably electrically connected to each other with high reliability. In Fig. 18, the conductive thin film 1104 and the device electrodes 1102 and 1103 are stacked in order of the substrate, device electrodes, and 5 conductive thin film from the bottom, but may be stacked in order of the substrate, conductive thin film, and device electrodes from the bottom.

The electron-emitting portion 1105 is a fissured portion formed in part of the conductive thin film 1104, 10 and has an electrically higher resistance than that of the peripheral conductive thin film. The fissure is formed by electrification forming processing (to be described later) in the conductive thin film 1104. In some cases, fine particles having a particle diameter of several Å to 15 several hundred Å are set in the fissure. As it is difficult to exactly illustrate the actual position and shape of the electron-emitting portion, Fig. 3 schematically show the electron-emitting portion.

The thin film 1113, which is made of carbon or a carbon 20 compound, covers the electron-emitting portion 1115 and its peripheral portion. The thin film 1113 is formed by electrification activation (to be described later) after electrification forming processing.

The thin film 1113 is preferably graphite 25 monocristalline, graphite polycristalline, amorphous carbon, or mixture thereof, and its thickness is 500 [Å]

or less, and more preferably 300 [Å] or less.

As it is difficult to exactly illustrate the actual position and shape of the thin film 1113, Fig. 3 schematically shows the thin film 1113. Fig. 3(a) shows 5 a device in which part of the thin film 1113 is removed.

The basic arrangement of the preferred device has been described.

In this electron-emitting device, the substrate 1101 is made of soda-lime glass, and the device electrodes 1102 10 and 1103 are formed from an Ni thin film. The thickness d of the device electrode is 1,000 [Å], and the electrode interval L is 2 [μ m].

The main material of the fine particle film is Pd or PdO. The fine particle film has a thickness of about 100 15 [Å] and a width W of 100 [Å].

Next, a method of manufacturing a preferred flat surface-conduction type emitting device will be described.

Figs. 19(a) to 19(d) are sectional views for explaining the steps in manufacturing the 20 surface-conduction type emitting device. The same reference numerals as in Fig. 18 denote the same parts.

As shown in Fig. 19(a), the device electrodes 1102 and 1103 are formed on the substrate 1101. In formation, the substrate 1101 is fully washed with a detergent, pure 25 water, and an organic solvent, and the device electrode material is deposited on the substrate 1101. (As the

deposition method, a vacuum film formation technique such as an evaporation method or sputtering method may be used.) The deposited electrode material is patterned by a photolithography etching technique into a pair of device 5 electrodes (1102 and 1103) shown in Fig. 19(a).

As shown in Fig. 19(b), the conductive thin film 1104 is formed. In formation, an organic metal solution is applied to the substrate in Fig. 19(a), dried, and baked to form a fine particle film. The fine particle film is 10 patterned into a predetermined shape by photolithography etching. The organic metal solution is an organic metal compound solution containing as a main element the fine particle material used for the conductive thin film. (More specifically, this embodiment uses Pd as a main element. 15 This embodiment uses a dipping method as a coating method, but may use another method such as a spinner method or spraying method.)

The film formation method of the conductive thin film made from the fine particle film is not limited to the 20 organic metal solution coating method used in the embodiment, but may be another method such as a vacuum evaporation method, sputtering method, or chemical vapor deposition method.

As shown in Fig. 19(c), a proper voltage is applied 25 between the device electrodes 1102 and 1103 from a forming power source 1110 to perform electrification forming

processing, thereby forming the electron-emitting portion 1105.

In electrification forming processing, electrification is done for the conductive thin film 1104 5 made from the fine particle film to properly damage, deform, or change in quality part of the conductive thin film 1104 so as to change it into a structure suitable for emitting electrons. An appropriate fissure is formed in the thin film at a portion of the conductive thin film made from the 10 fine particle film that has changed into a structure suitable for emitting electrons (i.e., electron-emitting portion 1105). After the electron-emitting portion 1105 is formed, the electrical resistance measured between the device electrodes 1102 and 1103 greatly increases, compared 15 to the electrical resistance before the electron-emitting portion 1105 is formed.

Fig. 21 shows an example of an appropriate voltage waveform applied from the forming power source 1110 in order to explain the electrification method in more detail. A 20 pulse-like voltage is preferable to a case wherein forming is done for the conductive thin film made from the fine particle film. As shown in Fig. 21, a triangular-wave pulse having a pulse width T_1 is continuously applied at a pulse interval T_2 . At this time, a peak value V_{pf} of the 25 triangular-wave pulse is sequentially increased. Further, a monitor pulse P_m for monitoring the formation status of

the electron-emitting portion 1105 is inserted between triangular-wave pulses at a proper interval, and a flowing current is measured by a galvanometer 1111.

More specifically, the peak value V_{pf} is increased
5 by 0.1 [V] every pulse at the pulse width T_1 of 1 [msec] and the pulse interval T_2 of 10 [msec] in a vacuum atmosphere of about 10^{-5} [torr]. The monitor pulse P_m is inserted every time five triangular-wave pulses are applied. To avoid any adverse influence on forming processing, a monitor pulse
10 voltage V_{pm} is set to 0.1 [V]. When the electrical resistance between the device electrodes 1102 and 1103 reaches 1×10^6 [Ω], i.e., a current measured by the galvanometer 1111 upon application of monitor pulses reaches 1×10^{-7} [A] or less, electrification for forming
15 processing ends.

Note that this method is preferable to the surface-conduction type emitting device of this embodiment. In case of changing the design of the surface-conduction type emitting device such as the material or thickness of
20 the fine particle film or the device electrode interval L , the electrification conditions are desirably changed in accordance with the changed design.

As shown in Fig. 19(d), a proper voltage is applied between the device electrodes 1102 and 1103 from an
25 activation power source 1112 to perform electrification activation processing so as to improve electron emission

characteristics.

Electrification activation processing is processing of performing electrification for the electron-emitting portion 1105 formed by electrification forming processing 5 under appropriate conditions, and depositing carbon or a carbon compound around the electron-emitting portion 1105. (In Fig. 19(d), a deposit of carbon or a carbon compound is illustrated as a material 1113.) Compared to an emission current before electrification activation processing, 10 electrification activation processing can increase an emission current typically 100 times or more at the same application voltage.

More specifically, a voltage pulse is periodically applied in a vacuum atmosphere of 10^{-4} to 10^{-5} [torr] to 15 deposit carbon or a carbon compound derived from an organic compound existing in the vacuum atmosphere. The deposit 1113 is graphite monocystalline, graphite polycystalline, amorphous carbon, or mixture thereof. The thickness of the accumulated material 1113 is 500 [\AA] or less, and more 20 preferably 300 [\AA] or less.

Fig. 21(a) shows an example of an appropriate voltage waveform applied from the activation power source 1112 in order to explain the electrification method in more detail. For example, a rectangular-wave voltage V_{ac} is 14 [V], a 25 pulse width T_3 is 1 [msec], and a pulse interval T_4 is 10 [msec]. These electrification conditions are preferable

to the surface-conduction type emitting device of this embodiment. In case of changing the design of the surface-conduction type emitting device, the electrification conditions are preferably changed in 5 accordance with the changed design.

Reference numeral 1114 shown in Fig. 19(d) denotes an anode electrode for capturing an emission current I_e emitted from the surface-conduction type emitting device. The anode electrode 1114 is connected to a DC high-voltage 10 power source 1115 and galvanometer 1116. (In case of performing activation processing after the substrate 1101 is incorporated in the display panel, the fluorescent surface of the display panel is used as the anode electrode 1114.)

15 While a voltage from the activation power source 1112 is applied, the galvanometer 1116 measures the emission current I_e , and monitors the progress of electrification activation processing to control the operation of the activation power source 1112. Fig. 6(b) shows an example 20 of the emission current I_e measured by the galvanometer 1116. As the activation power source 1112 starts applying a pulse voltage, the emission current I_e increases with the elapse of time, gradually comes into saturation, and hardly increases. When the emission current I_e substantially 25 saturates, application of the voltage from the activation power source 1112 is stopped to stop electrification

activation processing.

Note that these electrification conditions are preferable to the surface-conduction type emitting device of this embodiment. In case of changing the design of the 5 surface-conduction type emitting device, the conditions are preferably changed in accordance with the changed design.

In this manner, the flat surface-conduction type emitting device shown in Fig. 19(e) is manufactured.

10 (Stepped Surface-Conduction Type Emitting
Device)

Another typical arrangement of the surface-conduction type emitting device having an electron-emitting portion or its peripheral portion formed 15 from a fine particle film, i.e., a stepped surface-conduction type emitting device will be described.

Fig. 22 is a schematic sectional view for explaining the basic arrangement of the stepped surface-conduction type emitting device. In Fig. 22, reference numeral 1201 denotes a substrate; 1202 and 1203, device electrodes; 1206, a step-forming member; 1204, a conductive thin film using a fine particle film; 1205, an electron-emitting portion formed by electrification forming processing; and 1213, a thin film formed by electrification activation processing.

25 The stepped device is different from the flat device described above in that one of the device electrodes (1202)

is formed on the step-forming member 1206 and the conductive thin film 1204 covers the side surface of the step-forming member 1206. The device electrode interval L in Fig. 18 is set as a step height L_s of the step-forming member 1206 5 in the stepped device. The substrate 1201, device electrodes 1202 and 1203, and conductive thin film 1204 using the fine particle film can use the materials listed in the description of the flat device. The step-forming member 1206 uses an electrically insulating material such 10 as SiO_2 .

A method of manufacturing the stepped surface-conduction type emitting device will be described with reference to Fig. 23. Figs. 23(a) to 23(f) are sectional views for explaining the manufacturing steps. 15 The same reference numerals as in Fig. 22 denote the same parts.

As shown in Fig. 23(a), the device electrode 1203 is formed on the substrate 1201.

As shown in Fig. 23(b), an insulating layer for 20 forming the step-forming member is stacked. The insulating layer may be stacked by sputtering, e.g., SiO_2 , but may be formed by another film formation method such as a vacuum evaporation method or printing method.

As shown in Fig. 23(c), the device electrode 1202 is 25 formed on the insulating layer.

As shown in Fig. 23(d), part of the insulating layer

is etched away to expose the device electrode 1203.

As shown in Fig. 23(e), the conductive thin film 1204 using the fine particle film is formed. To form the film 1204, a film formation technique such as a coating method 5 is used similar to the flat device.

Similar to the flat device, electrification forming processing is performed to form an electron-emitting portion. (The same processing as electrification forming processing for the flat device described with reference to 10 Fig. 4(c) is performed).

Similar to the flat device, electrification activation processing is done to deposit carbon or a carbon compound around the electron-emitting portion. (The same processing as electrification activation processing for 15 the flat device described with reference to Fig. 4(d) is performed).

In this fashion, the stepped surface-conduction type emitting device shown in Fig. 23(f) is manufactured.

(Characteristics of Surface-Conduction Type
20 Electron-Emitting Device Used in Display Apparatus)

The characteristics of the surface-conduction type electron-emitting device used in the display apparatus will be described.

Fig. 24 shows typical examples of the (emission
25 current I_e) vs. (device application voltage V_f) characteristic and (device current I_f) vs. (device

application voltage V_f) characteristic of the device used in the display apparatus. The emission current I_e is much smaller than the device current I_f , and is difficult to illustrate by the same measure as the device current I_f .

5 In addition, these characteristics change when design parameters such as the size and shape of the device are changed. Thus, the two characteristics of the graph are illustrated in arbitrary units.

Regarding the emission current I_e , the device used
10 in the display apparatus has the following three
characteristics:

First, when a voltage equal to or higher than a given voltage (to be referred to as a threshold voltage V_{th}) is applied to the device, the emission current I_e drastically
15 increases. At a voltage lower than the threshold voltage V_{th} , almost no emission current I_e is detected.

In other words, the device is a nonlinear device with the clear threshold voltage V_{th} for the emission current I_e .

20 Second, the emission current I_e changes depending on the device application voltage V_f , so that the magnitude of the emission current I_e can be controlled by the voltage V_f .

Third, the current I_e emitted by the device at the
25 device application voltage V_f exhibits a high response speed. Hence, the charge amount of electrons emitted by

the device can be controlled by the application time of the voltage V_f .

The surface-conduction type emitting device having these characteristics can be preferably applied to the 5 display apparatus. For example, if a display apparatus having many devices in correspondence with the pixels of a display screen uses the first characteristic, the display screen is sequentially scanned to display an image. This means that the threshold voltage V_{th} or more is properly 10 applied to a device during driving in accordance with a desired emission luminance, whereas a voltage lower than the threshold voltage V_{th} is applied to an unselected device. By sequentially switching devices to be driven, the display screen can be sequentially scanned to display an image. 15 By using the second or third characteristic, the emission luminance can be controlled to realize tone level display.

As a supplemental remark of Fig. 24, the device current I_f has a nonlinear characteristic which projects 20 downward, similar to the emission current, but has a characteristic that a small current flows even at a voltage lower than the threshold current V_{th} .

(Structure of Multi Electron Beam Source With Many Devices Wired in Simple Matrix)

25 The structure of the multi electron beam source in which surface-conduction type emitting devices are

arranged on a substrate and wired in a simple matrix will be described.

Fig. 25 is a plan view of the multi electron beam source used in the display panel of Fig. 16.

5 Surface-conduction type emitting devices like the one shown in Fig. 18 are arranged on a substrate. These devices are wired in a simple matrix by the row-direction wiring electrodes 1003 and column-direction wiring electrodes 1004. At each intersection of the row-direction wiring electrode 1003 and column-direction wiring electrodes 1004, 10 an insulating layer (not shown) is formed between the electrodes to maintain electrical insulation.

Fig. 26 is a sectional view take along the line B - B' in Fig. 25.

15 A multi electron source having this structure is manufactured by forming in advance on the substrate the row-direction wiring electrodes 1003, and column-direction wiring electrodes 1004, insulating layers (not shown) between the electrodes, and the device electrodes and 20 conductive thin films of the surface-conduction type emitting device, and supplying power to respective devices via the row-direction wiring electrodes 1003 and column-direction wiring lines 1004 to perform 25 electrification forming processing and electrification activation processing.

Fig. 27 is a block diagram showing a display panel

using the surface-conduction type emitting device described above as an electron beam source.

In Fig. 27, reference numeral 2100 denotes a display panel; 2101, a driving circuit for the display panel; 2102, 5 a display controller; 2103, a multiplexer; 2104, a decoder; 2105, an I/O interface circuit; 2106, a CPU; 2107, an image generation circuit; 2108, 2109, and 2110, image memory interface circuits; 2111, an image input interface circuit; 2112 and 2113, TV signal reception circuits; and 2114, an 10 input portion. (When this display apparatus receives a signal containing both image information and audio information such as a TV signal, the apparatus displays the image information while reproducing the audio information. A description of a circuit or a speaker regarding reception, 15 division, reproduction, processing, storage, or the like of the audio information, which is not directly related to the features of the present invention, will be omitted.)

The functions of the respective units will be explained along the flow of an image signal.

20 The TV signal reception circuit 2113 is a circuit for receiving a TV image signal transmitted using a radio transmission system such as radio waves or spatial optical communication. The scheme of a TV signal to be received is not particularly limited, and can employ various schemes 25 such as the NTSC scheme, PAL scheme, and SECAM scheme. A TV signal (so-called high-quality TV signal of the MUSE

scheme or the like) realized by a larger number of scanning lines than the above-mentioned schemes is a preferable signal source to take the advantages of the display panel which can realize a large area and a large number of pixels.

5 The TV signal received by the TV signal reception circuit 2113 is output to the decoder 2104.

The TV signal reception circuit 2112 receives a TV image signal transmitted using a wire transmission system such as a coaxial cable or optical fiber. The scheme of 10 a TV signal to be received is not particularly limited, similar to the TV signal reception circuit 2113. The TV signal received by the circuit 2112 is also output to the decoder 2104.

The image input interface circuit 2111 is a circuit 15 for receiving an image signal supplied from an image input device such as a TV camera or image read scanner, and outputs the received image signal to the decoder 2104.

The image memory interface circuit 2110 is a circuit for receiving an image signal stored in a video tape 20 recorder (to be briefly referred to as a VTR hereinafter), and outputs the received image signal to the decoder 2104.

The image memory interface circuit 2109 is a circuit for receives an image signal stored in a video disk, and outputs the received image signal to the decoder 2104.

25 The image memory interface circuit 2108 is a circuit for receiving an image signal from a device such as a

so-called still image disk which stores still image data, and outputs the received still image data to the decoder 2104.

The I/O interface circuit 2105 is a circuit for 5 connecting the display apparatus to an external computer, computer network, or output device such as a printer. The I/O interface circuit 2105 allows inputting/outputting image data, character • graphic information, and in some cases allows inputting/outputting a control signal and 10 numerical data between the CPU 2106 of the display apparatus and an external device.

The image generation circuit 2107 generates display image data on the basis of image data or character • graphic information externally input via the I/O interface circuit 2105, or image data or character • graphic information 15 output from the CPU 2106. This circuit incorporates circuits necessary to generate images such as a programmable memory for storing image data and character • graphic information, a read-only memory storing image 20 patterns corresponding to character codes, and a processor for performing image processing. Display image data generated by the circuit is output to the decoder 2104. In some cases, display image data can also be output to an external computer network or printer via the I/O interface 25 circuit 2105.

The CPU 2106 mainly performs operation control of the

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display apparatus, and operations concerning generation, selection, and editing of display images.

For example, the CPU 2106 outputs a control signal to the multiplexer 2103 to properly select or combine image signals to be displayed on the display panel. At this time, the CPU 2106 generates a control signal to the display panel controller 2102 in accordance with an image signal to be displayed, and appropriately controls the operation of the display apparatus in terms of the screen display frequency, the scanning method (e.g., interlaced or non-interlaced scanning), the number of scanning lines for one frame, and the like. The CPU 2106 directly outputs image data or character • graphic information to the image generation circuit 2107. In addition, the CPU 2106 accesses an external computer or memory via the I/O interface circuit 2105 to input image data or character • graphic information.

The CPU 2106 may also be concerned with operations for other purposes. For example, the CPU 2106 can be directly concerned with the function of generating and processing information, like a personal computer or wordprocessor.

Alternatively, the CPU 2106 may be connected to an external computer network via the I/O interface circuit 2105 to perform operations such as numerical calculation in cooperation with the external device.

The input portion 2114 allows the user to input an

instruction, program, or data to the CPU 2106. As the input portion 2114, various input devices such as a joystick, bar code reader, and speech recognition device are available in addition to a keyboard and mouse.

5 The decoder 2104 is a circuit for inversely converting various image signals input from the circuits 2107 to 2113 into three primary color signals, or a luminance signal, I signal, and Q signal. As is indicated by the dotted line in Fig. 27, the decoder 2104 desirably 10 incorporates an image memory in order to process a TV signal of the MUSE scheme or the like which requires an image memory in inverse conversion. Using the image memory advantageously facilitates display of a still image, or image processing and editing such as thinning, 15 interpolation, enlargement, reduction, and synthesis of images in cooperation with the image generation circuit 2107 and CPU 2106.

The multiplexer 2103 appropriately selects a display image on the basis of a control signal input from the CPU 20 2106. More specifically, the multiplexer 2103 selects a desired image signal from inversely converted image signals input from the decoder 2104, and outputs the selected image signal to the driving circuit 2101. In this case, image signals can be selectively switched within a 1-frame 25 display time to display different images in a plurality of areas of one frame, like a so-called multiwindow

television.

The display panel controller 2102 is a circuit for controlling the operation of the driving circuit 2101 on the basis of a control signal input from the CPU 2106.

5 As the basic operation of the display panel, the display panel controller 2102 outputs, e.g., a signal for controlling the operation sequence of a driving power source (not shown) of the display panel to the driving circuit 2101.

10 As the display panel driving method, the display panel controller 2102 outputs, e.g., a signal for controlling the screen display frequency or scanning method (e.g., interlaced or non-interlaced scanning) to the driving circuit 2101.

15 In some cases, the display panel controller 2102 outputs to the driving circuit 2101 a control signal concerning adjustment of the image quality such as the luminance, contrast, color tone, or sharpness of a display image.

20 The driving circuit 2101 is a circuit for generating a driving signal to be applied to the display panel 2100, and operates based on an image signal input from the multiplexer 2103 and a control signal input from the display panel controller 2102.

25 The functions of the respective units have been described. With the arrangement shown in Fig. 12, the

display apparatus can display pieces of image information input from various image information sources on the display panel 2100.

More specifically, various image signals of 5 television broadcasting and the like are inversely converted by the decoder 2104, properly selected by the multiplexer 2103, and input to the driving circuit 2101. The display controller 2102 generates a control signal for controlling the operation of the driving circuit 2101 in 10 accordance with an image signal to be displayed. The driving circuit 2101 applies a driving signal to the display panel 2100 on the basis of the image signal and control signal.

As a result, an image is displayed on the display panel 15 2100.

A series of operations are systematically controlled by the CPU 2106.

This display apparatus can simply display an image selected from a plurality of pieces of image information 20 with the image memory incorporated in the decoder 2104, the image generation circuit 2107, and the CPU 2106. In addition, the display apparatus can perform, for image information to be displayed, image processing such as enlargement, reduction, rotation, movement, edge 25 enhancement, thinning, interpolation, color conversion, and conversion of the aspect ratio of an image, and image

editing such as synthesis, erase, connection, exchange, and pasting. Although not mentioned in this embodiment, a dedicated circuit for processing and editing audio information may be adopted, similar to image processing and 5 image editing.

The display apparatus can function as a display device for television broadcasting, a terminal device for video conferences, an image editing device for processing still images and dynamic images, a terminal device for a 10 computer, an office terminal device such as a wordprocessor, a game device, and the like. This display apparatus can be variously applied for industrial and business purposes.

Fig. 27 merely shows an example of the arrangement of the display apparatus using the display panel having a 15 surface-conduction type emitting device as an electron beam source. The present invention is not limited to this. For example, a circuit associated with a function unnecessary for the application purpose may be eliminated from the building elements in Fig. 27. To the contrary, another 20 building element may be added in accordance with the application purpose. For example, when the display apparatus is used as a television telephone set, transmission and reception circuits including a television camera, audio microphone, lighting, and modem are 25 preferably added to the building elements.

The display panel using particularly a

surface-conduction type emitting device as an electron beam source can be easily made thin in the display apparatus, which can reduce the depth of the whole display apparatus. In addition, the display panel using a surface-conduction type emitting device as an electron beam source easily implements a large screen, and exhibits high luminance and wide view angle. Accordingly, this display apparatus can display an impressive image with reality and high visibility.

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INDUSTRIAL APPLICABILITY

The present invention can suppress an erroneous display and suppress degradation in characteristics in executing power-on, power-off, and emergency power source shutdown sequences for an image display apparatus.

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